



SUBSTITUTE SPECIFICATION

TITLE OF THE INVENTION

SOLID-STATE IMAGE SENSING APPARATUS

BACKGROUND OF THE INVENTION

5 (1) Field of the Invention

This invention relates to a solid-state image sensing apparatus, and particularly to a solid-state image sensing apparatus that can photograph a moving object with no distortion.

10 (2) Description of the Related Art

FIG. 1 is a diagram showing a hardware configuration of a general Metal Oxide Semiconductor (MOS) type solid-image sensing apparatus. As is shown in FIG. 1, the solid-state image sensing apparatus 110 includes a pixel unit 112, a row scanning shift register 114, a noise cancellation unit 116, a column scanning shift register 118, an output amplifier 120 and a plurality of timing generation circuits (not illustrated).

In the pixel unit 112, a plurality of pixels (for example, a pixel 112a and a pixel 112b) are laid out two-dimensionally. Each pixel performs a photoelectric conversion, converts inputted light into an electric signal and outputs the electric signal.

The row scanning shift register 114 is a shift register which is composed of the same number of rows of bits as the rows of pixels laid out in the pixel unit 112. Each bit corresponds to each row of the pixel unit 112 one for one. It is indicated that when a bit value of the shift register corresponding to each row is 1 (the potential is at a High level), the pixels of the column are selected; when the bit value is 0 (the potential is at a Low level), the pixels of the column are not selected.

The noise cancellation unit 116 performs noise reduction of electric signals of one row's pixels transmitted through a vertical signal line.

The column scanning shift resistor 118 shifts electric signals of one row passed through the noise cancellation unit 116 in the right direction and outputs the electric signals pixel by pixel.

The output amplifier 120 amplifies and outputs the electric signals outputted from the column scanning shift resistor 118.

The timing generation circuit is set up for each row, generates various signals, and provides each pixel with the signals. The timing generation circuit is explained in detail later.

FIG. 2 is a circuit diagram of each pixel that composes the pixel unit 112 (for example, the pixel 112a and the pixel 112b). As is shown in FIG. 2, each pixel includes a photodiode (hereinafter, referred to as "PD") 122, a MOS-type readout transistor 124, a MOS-type reset transistor 126, a MOS-type signal detection region 128, an amplifier transistor 130, a row selection transistor 132 and a MOS-type load transistor 133.

The PD 122 performs an electric conversion of incident light and accumulates electric charge. The readout transistor 124 reads out the electric charge accumulated in the PD 122 in response to a pulse of a PD readout signal generated by the timing generation circuit.

The signal detection region 128 accumulates the readout electric charge temporarily. The reset transistor 126 initializes the potential of the signal detection region 128 to the potential of a drain voltage signal VDD in response to a pulse of a detection region reset signal generated by the timing generation circuit.

The amplifier transistor 130 receives, as a gate voltage, the voltage in proportion to the electric charge of PD 122 that has passed the readout transistor 124 and that is accumulated in the signal detection region 128, and lets the current in proportion to the gate voltage pass through.

The row selection transistor 132 outputs the electric current that has passed the amplifier transistor 130 to the vertical signal

line in response to a pulse of the row selection signal generated by the timing generation circuit.

FIG. 3 is a circuit diagram showing an example of a timing generation circuit. As is described above, a timing generation circuit 140 is set up for each row of the pixel unit 112. The timing generation circuit 140 shown in FIG. 3 includes MOS-type transistors 142, 144, 148 and 152; bootstrap circuits 146 and 150.

Each of the transistors 142 and 144 receives a multiplexer precharge signal VDRRS in the gate and lets the output of the row scanning shift register 114 pass through when the multiplexer precharge signal VDRRS reaches the High level.

Each of the bootstrap circuits 146 and 150 is configured by connecting a drain and a source of an NMOS-type transistor and fulfills a function as a capacitor that accumulates electric charge by applying potential to the gate. The output voltage of the row scanning shift register 114 that has passed through the transistor 142 is applied to the gate of the bootstrap circuit 146. The output voltage of the row scanning shift register 114 that has passed through the transistor 144 is applied to the gate of the bootstrap circuit 150.

The transistor 148 is an NMOS-type transistor. Its gate is connected to the bootstrap circuit 146, and its drain is connected to the drain and the source of the bootstrap circuit 146. When the electric charge is accumulated in the bootstrap circuit 146 and the bootstrap circuit 146 becomes charged, voltage of the gate potential of the transistor 148 rises. Therefore, when the bootstrap circuit 146 becomes charged, the gate potential of the transistor 148 further rises because of a detection region reset signal RSCCELL inputted from the drain of the transistor 148, wherein the detection region reset signal RSCCELL passes through the source without voltage drop. The detection region reset signal RSCCELL, which has passed through the source of the transistor 148, is applied to the

gate of the reset transistor 126 of each pixel in a row assigned to the timing generation circuit 140.

The transistor 152 is an NMOS-type transistor. Its gate is connected to the bootstrap circuit 150, and its drain is connected to the drain and the source of the bootstrap circuit 150. When the electric charge is accumulated in the bootstrap circuit 150 and the bootstrap circuit 150 becomes charged, voltage of the gate potential of the transistor 152 rises. Therefore, when the bootstrap circuit 150 becomes charged, the gate potential of the transistor 152 further rises because of a PD readout signal TRANS inputted from the drain of the transistor 152, wherein the PD readout signal TRANS passes through the source without voltage drop. The PD readout signal TRANS, which has passed the source of the transistor 152, is applied to the gate of the readout transistor 124 of each pixel in a row assigned to the timing generation circuit 140.

FIG. 4 is a timing diagram of the timing generation circuit 140 shown in FIG. 3. The timing diagram shown in FIG. 4 indicates timings of signals of a certain row (the "n"th row) and the next row (the "n+1"th row).

Focusing attention on the "n"th row, when output of the row scanning shift register 114 reaches the High level, a pulse of the multiplexer precharge signal VDRRS at the High level is applied to the gates of the transistors 142 and 144 for a predetermined time. During the predetermined time, electric charge is accumulated in the bootstrap circuits 146 and 150, and the bootstrap circuits 146 and 150 become charged. After that, a pulse of the detection region reset signal RSCCELL passes through the transistor 148 and is applied to the gate of the reset transistor 126 of each pixel shown in FIG. 2. Then, the potential of the signal detection region 128 is initialized to the potential of the drain voltage signal VDD. After that, a pulse of a PD readout signal TRANS passes through the transistor 152 and is applied to the gate of the readout transistor

124 of each pixel. Then, the electric charge accumulated in the PD 122 is read out, passes through the readout transistor 124 and is accumulated in the signal detection region 128.

At this time, the electric charge accumulated in the PD 122
5 has been discharged. Therefore, accumulation of electric charge to the PD 122 starts at the trailing edge of a pulse of the PD readout signal TRANS.

On the other hand, when output of the row scanning shift register 114 becomes the Low level, a pulse of a multiplexer
10 precharge signal VDRRS is applied to the transistors 142 and 144. Hereby, the electric charge accumulated in bootstrap circuits 146 and 150 is discharged.

After that, a shift by one bit of the value held in the row scanning shift register 114 causes the timing generation circuit 140
15 for the "n+1"th row to generate a similar signal. Likewise, the PD 122 of each pixel in the "n+1"th row starts to accumulate electric charge.

Again, focusing attention on the "n"th row, the timing generation circuit 140 outputs a similar signal described above at a
20 phase where output of the row scanning shift register 114 becomes the High level. When a pulse of a PD readout signal TRANS passes through the transistor 152 and is applied to the gate of the readout transistor 124, the electric charge that has been accumulated in the PD 122 is read out, passes through the transistor 124 and is
25 accumulated in the signal detection region 128. By applying the potential of the signal detection region 128 to the amplifier transistor 130, the electric current in proportion to the accumulated electric charge of the PD 122 passes through the amplifier transistor 130. At this time, a row selection signal (not illustrated in FIG. 3
30 and FIG. 4) is applied to the row selection transistor 132 and the electric current flows in the load transistor 133 through a vertical signal line. The voltage of the vertical line at this time is inputted

into the noise cancellation unit 116.

In other words, time T3 for accumulating the electric charge to the PD 122 is the time from the trailing edge of a pulse of a PD readout signal TRANS until the leading edge of the next pulse.

5 As is described above, a conventional solid-state image sensing apparatus accumulates electric charge for each row, shifting a value held by the row scanning shift register 114 in sequence, and takes a photograph of an object. (For example, refer to Japanese Laid-Open Patent application No. 08-182005.)

10 However, the conventional solid-state image sensing apparatus accumulates electric charge to a PD by shifting every row. Thus, there is a problem that a photograph has a distortion when a photograph of a moving object is taken.

This problem is explained using the figures. FIG. 5 is a
15 diagram to explain a gap of electric charge accumulation time for each row. The solid-state image sensing apparatus 110 starts to accumulate electric charge for every row in sequence in a vertical scanning direction using output of the row scanning shift register 114 and detects accumulated electric charge for every row in
20 sequence after the time T3 has passed. As is described above, the start timing for accumulating electric charge is different for each row. Therefore, it is possible to take a photograph with no distortion as shown in FIG. 6A when a stationary object such as a car that is not moving is photographed. But a photograph has a distortion as
25 shown in FIG. 6B when a moving object such as a moving car is photographed.

SUMMARY OF THE INVENTION

Accordingly, the present invention is available to solve the
30 above-noted problem and it is the object of the present invention to provide a solid-state image sensing apparatus that makes it possible to take a photograph of a moving object with no distortion.

In order to achieve the above-mentioned object, the solid-state image sensing apparatus according to the present invention is a solid-state image sensing apparatus that performs photoelectric conversion of incident light, comprising: a
5 photosensitive unit in which a plurality of photoelectric conversion circuits are laid out one-dimensionally or two-dimensionally, each of the photoelectric conversion circuits corresponding to a pixel and including a photodiode that accumulates electric charge by performing the photoelectric conversion of incident light and an
10 output circuit that outputs the accumulated electric charge as an electric signal; an electric charge simultaneous removal unit operable to simultaneously remove the accumulated electric charge in the photodiodes laid out in a predetermined region to be read out in the photosensitive unit; and an electric charge accumulation
15 unit operable to accumulate electric charge in the photodiode laid out in the region to be read out during a predetermined time after the accumulated electric charge in the photodiode that is laid out in the region is removed.

This configuration makes it possible to remove
20 simultaneously accumulated electric charge in the photodiode laid out in the predetermined region to be read out in the photosensitive unit. Consequently, it is possible to start simultaneously and end simultaneously electric charge accumulation to the photodiode laid out in the region to be read out. Therefore, it is possible to
25 photograph a moving object with no distortion.

For example, it is acceptable that the electric charge accumulation unit generates an electric accumulation start signal to start electric charge accumulation to the photodiode laid out in the region to be read out.

30 This configuration makes it possible to control the start of electric charge accumulation based on the electric signal.

Additionally, it is satisfactory that the solid-state image

sensing apparatus further comprises an incident light control unit operable to control incidence of light into the photosensitive unit, wherein the electric charge accumulation unit starts incidence of light to the photosensitive unit using the incident light control unit
5 after the electric charge simultaneous removal unit simultaneously removes the accumulated electric charge to the photodiode laid out in the region to be read out.

This configuration makes it possible to control the start of electric charge accumulation by a mechanical method such as a
10 shutter.

Preferably, it is acceptable that the solid-state image sensing apparatus further comprises an electric signal readout unit operable to read out the electric signal outputted from the photoelectric conversion circuit laid out in the region to be read out, and that the
15 electric signal readout unit reads out simultaneously accumulated electric charge of the photodiode laid out in the region to be read out.

Hereby, it is possible to provide a solid-state image sensing apparatus that operates at a high speed.

The camera according to another aspect of the present invention is a camera that photographs an object comprising a solid-state image sensing apparatus; and a mechanical shutter, wherein the solid-state image sensing apparatus includes: a photosensitive unit in which a plurality of photoelectric conversion
20 circuits are laid out one-dimensionally or two-dimensionally, each of the photoelectric conversion circuits corresponding to a pixel and including a photodiode that accumulates electric charge by performing the photoelectric conversion of incident light and an output circuit that outputs the accumulated electric charge as an
25 electric signal; an electric charge simultaneous removal unit operable to simultaneously remove the accumulated electric charge in the photodiode laid out in a predetermined region to be read out
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in the photosensitive unit; an electric charge accumulation unit operable to accumulate electric charge in the photodiode laid out in the region to be read out during a predetermined time after accumulated electric charge in the photodiode that is laid out in the region is removed; and an incident light control unit operable to control incidence of light into the photosensitive unit, wherein the mechanical shutter is set up between the photosensitive unit of the solid-state image sensing apparatus and an object to be photographed, the electric charge accumulation unit ends electric charge accumulation to the photodiode laid out in the region to be read out using the incident light control unit by blocking out incidence of light into the photosensitive unit, and the incident light control unit controls incidence of light into the photosensitive unit by controlling opening and shutting of the mechanical shutter.

This configuration makes it possible to remove simultaneously accumulated electric charge in the photodiode laid out in the predetermined region to be read out in the photosensitive unit. Consequently, it is possible to start simultaneously and end simultaneously electric charge accumulation to the photodiode laid out in the region to be read out. Therefore, it is possible to photograph a moving object with no distortion.

The image sensing method according to yet another aspect of the present invention is an image sensing method for photographing an object using a solid-state sensing apparatus, wherein the solid-state image sensing apparatus includes a photosensitive unit in which a plurality of photoelectric conversion circuits are laid out one-dimensionally or two-dimensionally, each of the photoelectric conversion circuits corresponding to a pixel and including a photodiode that accumulates electric charge by performing the photoelectric conversion of incident light and an output circuit that outputs the accumulated electric charge as an electric signal, and the image sensing method comprising the steps of: simultaneously

removing the accumulated electric charge in the photodiode laid out in a predetermined region to be read out in the photosensitive unit; and accumulating electric charge in the photodiode laid out in the region to be read out during a predetermined time after the
5 accumulated electric charge of the photodiode that is laid out in the region is removed.

This method makes it possible to remove simultaneously accumulated electric charge in the photodiode laid out in the predetermined region to be read out in the photosensitive unit.
10 Consequently, it is possible to start simultaneously and end simultaneously electric charge accumulation to the photodiode laid out in the region to be read out. Therefore, it is possible to photograph a moving object with no distortion.

As further information about technical background to this
15 application, Japanese patent application No. 2003-092487 filed on March 28, 2003 is incorporated herein by reference.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other subjects, advantages and features of the
20 invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings that illustrate a specific embodiment of the invention. In the Drawings:

FIG. 1 is a diagram showing a hardware configuration of a general MOS type solid-image sensing apparatus;

25 FIG. 2 is a circuit diagram of each pixel that composes the pixel unit;

FIG. 3 is a circuit diagram showing an example of a timing generation circuit;

FIG. 4 is a timing diagram of the timing generation circuit
30 shown in FIG. 3;

FIG. 5 is a diagram to explain a gap of electric charge accumulation time for each row;

FIG. 6A is a diagram showing an example of a picture obtained by photographing a stationary object;

FIG. 6B is a diagram showing an example of a picture obtained by photographing a moving object;

5 FIG. 7 is a circuit diagram showing an example of a timing generation circuit according to the First Embodiment;

FIG. 8 is a timing diagram of the timing generation circuit shown in FIG. 7;

10 FIG 9 is a circuit diagram showing an example of a timing generation circuit according to the Second Embodiment;

FIG. 10 is a circuit diagram of each pixel that composes the pixel unit according to the Second Embodiment;

FIG. 11 is a timing diagram of the timing generation circuit shown in FIG. 10;

15 FIG. 12 is a diagram showing another example of timing of the timing generation circuit shown in FIG 7;

FIG. 13 is a diagram explaining a start and an end of electric charge accumulation according to the First and Second Embodiments;

20 FIG. 14 is a diagram explaining another example of the start and the end of electric charge accumulation;

FIG. 15 is a diagram explaining yet another example of the start and the end of electric charge accumulation;

25 FIG. 16 is a diagram explaining still another example of the start and the end of electric charge accumulation;

FIG. 17(a) is a diagram showing a timing of opening and closing of the mechanical shutter;

FIG. 17(b) is a diagram showing a PD readout signal TRANS;

30 Each of FIG. 17(c)~FIG. 17(f) is a diagram showing a detection region reset signal RSCELL;

FIG. 18A is a diagram showing the pixel unit of the solid-state image sensing apparatus in the front part of which a mechanical

shutter is set up;

FIG. 18B is a diagram showing the pixel unit of the solid-state image sensing apparatus in the front part of which a liquid crystal shutter is set up;

5 FIG. 18C is a diagram showing the pixel unit of the solid-state image sensing apparatus in the front part of which nothing is set up; and

FIG. 19 is a diagram showing an equivalent circuit to a timing generation circuit using a CMOS-type transistor.

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DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

(The First Embodiment)

15 The hardware configuration of a MOS-type solid-state sensing apparatus according to the First Embodiment of the present invention is similar to the hardware configuration of the conventional solid-state sensing apparatus 110 explained in reference to FIG. 1. Therefore, its detailed explanation is not repeated here. However, the hardware configuration of a plurality
20 of timing generation circuits which is not illustrated in FIG. 1 is different from the conventional hardware configuration.

By the way, in front of the pixel unit 112 of the solid-state image sensing apparatus 110 according to the present embodiment, a mechanical shutter (not illustrated) and a mechanical shutter
25 control unit (not illustrated) are set up, wherein incidence of light to the pixel unit 112 is controlled by opening and shutting of the mechanical shutter.

A hardware configuration of each pixel that composes the pixel unit 112 is similar to the hardware configuration explained in
30 reference to FIG. 2. Therefore, its detailed explanation is not repeated here.

FIG. 7 is a circuit diagram showing an example of a timing

generation circuit. The timing generation circuit 30 is set up for each row of the pixel unit 112. The timing generation circuit 30 shown in FIG. 7 includes MOS-type transistors 32, 34, 36, 40, 42 and 46; and bootstrap circuits 38 and 44.

5 Each of the transistors 32 and 34 receives a multiplexer precharge signal VDRRS in the gate and lets the output of the row scanning shift register 114 pass through when the potential of the multiplexer precharge signal VDRRS reaches the High level.

10 Each of the transistors 36 and 42 receives an all pixel reset switch signal ALLRSSW in the gate and lets an all pixel reset signal ALLRSCLK pass through when the all pixel reset switch signal ALLSSW reaches the High level.

15 Each of the bootstrap circuits 38 and 44 is configured by connecting a drain and a source of an NMOS-type transistor and fulfills a function as a capacitor that accumulates electric charge by applying potential to the gate. To the gate of the bootstrap circuit 38 is applied: the output voltage of the row scanning shift register 114 that has passed through the transistor 32 or the all pixel reset signal ALLRSCLK that has passed through the transistor 36. To the
20 gate of the bootstrap circuit 44 is applied: the output voltage of the row scanning shift register 114 that has passed through the transistor 34 or the all pixel reset signal ALLRSCLK that has passed through the transistor 42.

25 The transistor 40 is an NMOS-type transistor. Its gate is connected to the bootstrap circuit 38, and its drain is connected to the drain and the source of the bootstrap circuit 38. When the electric charge is accumulated in the bootstrap circuit 38 and the bootstrap circuit 38 becomes charged, voltage of the gate potential of the transistor 40 rises. Therefore, when the bootstrap circuit 38
30 becomes charged, the gate potential of the transistor 40 further rises because of a detection region reset signal RSCCELL inputted from the drain of the transistor 40, wherein the detection region

reset signal RSCCELL passes through the source without voltage drop. The detection region reset signal RSCCELL, which has passed the source of the transistor 40, is applied to the gate of the reset transistor 126 of each pixel in a row assigned to the timing generation circuit 30.

The transistor 46 is an NMOS-type transistor. Its gate is connected to the bootstrap circuit 44, and its drain is connected to the drain and the source of the bootstrap circuit 44. When the electric charge is accumulated in the bootstrap circuit 44 and the bootstrap circuit 44 becomes charged, voltage of the gate potential of the transistor 46 rises. Therefore, when the bootstrap circuit 44 becomes charged, the gate potential of the transistor 46 further rises because of a PD readout signal TRANS inputted from the drain of the transistor 46, wherein the PD readout signal TRANS passes through the source without voltage drop. The PD readout signal TRANS, which has passed through the source of the transistor 46, is applied to the gate of the readout transistor 124 of each pixel in a row assigned to the timing generation circuit 30.

FIG. 8 is a timing diagram of the timing generation circuit 30. The timing diagram shown in FIG. 8 indicates timings of signals of a certain row (the "n"th row) and the next row (the "n+1"th row).

Focusing attention on the "n"th row, when the all pixel reset signal ALLRSCLK reaches the High level, a pulse of the all pixel reset switch signal ALLRSSW at the High level is applied to the gates of the transistors 36 and 42 for a predetermined time. During the predetermined time, electric charge is accumulated in the bootstrap circuits 38 and 44, and the bootstrap circuits 38 and 44 become charged.

After that, a pulse of a PD readout signal TRANS passes through the transistor 46 and is applied to the gate of the readout transistor 124 of each pixel shown in FIG. 2. Then, the electric charge accumulated in the PD 122 is read out, passes through the

transistor 124 and is accumulated in the signal detection region 128. At this time, the electric charge accumulated in the PD 122 has been discharged.

Additionally, a pulse of a detection region reset signal RSCCELL passes through the transistor 40 at the same time with a pulse of a PD readout signal TRANS and is applied to the gate of the reset transistor 126 of each pixel. Then, the potential of the signal detection region 128 is initialized to the potential of the drain voltage signal VDD.

Moreover, at the trailing edge of a pulse of a PD readout signal TRANS, a mechanical shutter is open (OPEN state). Therefore, accumulation of electric charge to the PD 122 starts at the trailing edge of a pulse for a PD readout signal TRANS and ends at the time when the mechanical shutter is closed. This duration is time T3, electric charge accumulation time to PD 122.

Additionally, after the trailing edge of pulse of an all pixel reset switch signal ALLSSW, the all pixel reset signal ALLRSCLK is made to be the Low level. Further, after the trailing edges of a detection region reset signal RSCCELL and a PD readout signal TRANS and at the time when an all pixel reset signal ALLRSCLK is the Low level, a pulse of the all pixel reset switch signal ALLSSW is applied to the gates of the transistors 36 and 42. Hereby, the electric charge accumulated in bootstrap circuits 38 and 44 is discharged.

By the way, the detection region reset signal RSCCELL, the PD readout signal TRANS, the all pixel reset switch signal ALLSSW and the all pixel reset signal ALLRSCLK, which are explained above, are the same in the timing generation circuits 30 of all the rows.

Therefore, it is configured so that the start timing and the end timing of time T3, the electric charge accumulation time to the PD 122 agree in all the pixels in the pixel unit 112.

After time T3, the electric charge accumulation time to the PD 122 has passed, and the electric charge accumulated in the PD 122

is read out row-by-row by shifting the value of the row scanning shift register 114 in sequence.

When output of the row scanning shift register 114 of the "n"th row reaches the High level, a pulse of the multiplexer precharge signal VDRRS at the High level is applied to the gates of the transistors 32 and 34 for a predetermined time. During the predetermined time, electric charge is accumulated in the bootstrap circuits 38 and 44, and the bootstrap circuits 38 and 44 become charged. After that, a pulse of the detection region reset signal RSCELL passes through the transistor 40 and is applied to the gate of the reset transistor 126 of each pixel shown in FIG. 2. Then, the potential of the signal detection region 128 is initialized to the potential of the drain voltage signal VDD. After that, a pulse of a PD readout signal TRANS passes through the transistor 46 and is applied to the gate of the readout transistor 124 of each pixel. Then, the electric charge accumulated in the PD 122 is read out, passes through the readout transistor 124 and is accumulated in the signal detection region 128. By applying the potential of the signal detection region 128 to the amplifier transistor 130, the electric current in proportion to the accumulated electric charge of the PD 122 passes through the amplifier transistor 130. At the time, a row selection signal (not illustrated in FIG. 7 and FIG. 8) is applied to the row selection transistor 132 and the electric current flows into the load transistor 133 through a vertical signal line. The voltage of the vertical line at this time is inputted into the noise cancellation unit 116.

After noise reduction is performed in the noise cancellation unit 116 to electric current inputted to the noise cancellation unit 116 in proportion to the "n"th row of the PD 122, the electric current is outputted pixel-by-pixel from the output amplifier 120 through the column scanning shift resistor 118.

When output of the row scanning shift register 114 becomes

the Low level, a pulse of a multiplexer precharge signal VDRRS is applied to the transistors 32 and 44. Hereby, the electric charge accumulated in bootstrap circuits 38 and 44 is discharged.

When readout of the pixels in the "n"th row has finished,
5 similar readout of the pixels of the "(n+1)"th row is performed. In this way, the readout of the pixels is performed row-by-row from the first row through the last row.

As is described above, according to the First Embodiment, a mechanical shutter is left to be open; and a pulse of a PD readout
10 signal TRANS is applied to the gates of the readout transistors 124 of all the pixels at the same time. Hereby, the electric charge accumulated in the PDs 122 of all the pixels is discharged at the same time; from the instant, the accumulation of electric charge to the PDs 122 starts. Additionally, the accumulation of electric
15 charge to the PDs 122 ends for the all pixels at the same time by closing the mechanical shutter. Therefore, the start timing and the end timing of the accumulation of electric charge to the PDs 122 for all the pixels agree. Consequently, it is possible to take a photograph with no distortion even if the object is moving.

20

(The Second Embodiment)

Next, a MOS-type solid-state image sensing apparatus according to the Second Embodiment of the present invention is explained. The hardware configuration of the MOS-type solid-state
25 sensing apparatus according to the Second Embodiment of the present invention is similar to the hardware configuration of the conventional solid-state sensing apparatus 110 explained in reference to FIG. 1. Therefore, its detailed explanation is not repeated here. However, the configuration of each pixel (for
30 example, pixel 112a and the pixel 112b) is different from the conventional configuration. Additionally, the hardware configuration of a plurality of timing generation circuits which is not

illustrated in FIG. 1 is different from the conventional hardware configuration.

By the way, in front of the pixel unit 112 of the solid-state image sensing apparatus 110 according to the present embodiment, similarly to the solid-state image sensing apparatus 110 according to the First Embodiment, a mechanical shutter (not illustrated) is set up and incidence of light to the pixel unit 112 is controlled by opening and shutting of the mechanical shutter.

FIG. 9 is a circuit diagram of each pixel that composes the pixel unit 112. As is shown in FIG. 9, each pixel 60 includes a PD 64, a MOS-type reset transistor 62, a MOS-type amplifier transistor 66, a MOS-type row selection transistor 68 and a MOS-type load transistor 69.

The PD 64 performs an electric conversion of incident light and accumulates electric charge.

The reset transistor 62 discharges the electric charge accumulated in the PD 64 in response to a pulse of a PD reset signal generated by the timing generation circuit.

The amplifier transistor 66 receives, as gate voltage, the voltage in proportion to the electric charge that is accumulated in the PD64 and lets the current in proportion to the gate voltage pass through.

The row selection transistor 68 outputs the electric current that has passed the amplifier transistor 66 to the vertical signal line in response to a pulse of the row selection signal generated by the timing generation circuit.

FIG. 10 is a circuit diagram showing an example of a timing generation circuit. The timing generation circuit 30 is set up for each row of the pixel unit 112. The timing generation circuit 30 shown in FIG. 10 has a similar hardware configuration to the hardware configuration of the timing generation circuit 30 shown in FIG. 7. However, a row selection signal SELECT is used instead of a

PD readout signal TRANS; and a PD reset signal RSCELL2 is used instead of a detection region reset signal RSCELL. Therefore, signals outputted by the transistors 40 and 46 are different from those of the First Embodiment. The other components of the configuration are similar to those of the timing generation circuit 30 shown in FIG. 7. Therefore, its detailed explanation is not repeated here.

The transistor 40 performs similar actions to the transistor 40 shown in FIG. 7 but a PD reset signal RSCELL2, which has passed the source of the transistor 40, is applied to the gate of the reset transistor 62 of the pixel 60 in a row assigned to the timing generation circuit 30.

The transistor 46 performs similar actions to the transistor 40 shown in FIG. 7 but the row selection signal SELECT, which has passed the source of the transistor 40, is applied to the gate of the row selection transistor 68 of the pixel 60 in a row assigned to the timing generation circuit 30.

FIG. 11 is a timing diagram of the timing generation circuit 30. The timing diagram shown in FIG. 11 indicates timings of signals of a certain row (the "n"th row) and the next row (the "n+1"th row).

Focusing attention on the "n"th row, when the all pixel reset signal ALLRSCLK reaches the High level, a pulse of the all pixel reset switch signal ALLRSSW at the High level is applied to the gates of the transistors 36 and 42 for a predetermined time. During the predetermined time, electric charge is accumulated in the bootstrap circuits 38 and 44, and the bootstrap circuits 38 and 44 become charged.

After that, a pulse of a PD reset signal RSCELL2 passes through the transistor 40 and is applied to the gate of the reset transistor 62 of each pixel 60 shown in FIG. 9. Then, the electric charge accumulated in the PD 64 is discharged.

At the trailing edge of a pulse of a PD reset signal RSCELL2, a

mechanical shutter is open. Therefore, accumulation of electric charge to the PD 64 starts at the trailing edge of a pulse of a PD reset signal RSCCELL2 and ends at the time when the mechanical shutter is closed. This duration is time T3, electric charge accumulation time to PD64.

Additionally, after the trailing edge of pulse of an all pixel reset switch signal ALLSSW, the all pixel reset signal ALLRCLK is made to be the Low level. Further, after the trailing edges of a PD reset signal RSCCELL2 and at the time when an all pixel reset signal ALLRCLK is the Low level, a pulse of the all pixel reset switch signal ALLSSW is applied to the gates of the transistors 36 and 42. Hereby, the electric charge accumulated in bootstrap circuits 38 and 44 is discharged.

By the way, the PD reset signal RSCCELL2, the all pixel reset switch signal ALLSSW and the all pixel reset signal ALLRCLK, which are explained above, are same in the timing generation circuits 30 of all the rows.

Therefore, it is configured so that the start timing and the end timing of time T3, the electric charge accumulation time to the PD 64 agree in all the pixels 60 in the pixel unit 112.

After time T3 for accumulating electric charge to the PD 64 has passed, the electric charge accumulated in the PD 64 is read out row-by-row by shifting the value of the row scanning shift register 114 in sequence.

When output of the row scanning shift register 114 of the "n"th row reaches the High level, a pulse of the multiplexer precharge signal VDRRS at the High level is applied to the gates of the transistors 32 and 34 for a predetermined time. During the predetermined time, electric charge is accumulated in the bootstrap circuits 38 and 44, and the bootstrap circuits 38 and 44 become charged. After that, a pulse of the row selection signal SELECT passes through the transistor 46 and is applied to the gate of the row

selection transistor 68 of each pixel 60 shown in FIG. 9. Since voltage in proportion to accumulated electric charge to PD 64 is applied to the gate of the amplifier transistor 66, electric current in proportion to accumulated electric charge to PD 64 passes through the amplifier transistor 66. Therefore, the row selection signal SELECT is applied to the gate of the row selection transistor 68. As a result, electric current in proportion to accumulated electric charge of PD 64 passes through the row selection transistor 68 and flows into the load transistor 69 through a vertical signal line. The voltage of the vertical line at this time is inputted into the noise cancellation unit 116.

After noise reduction is performed in the noise cancellation unit 116 to electric current inputted to the noise cancellation unit 116 in proportion to the "n"th row of the PD 122, the electric current is outputted pixel-by-pixel from the output amplifier 120 through the column scanning shift resistor 118.

When output of the row scanning shift register 114 becomes the Low level, a pulse of a multiplexer precharge signal VDRRS is applied to the transistors 32 and 34. Hereby, the electric charge accumulated in bootstrap circuits 38 and 44 is discharged.

When readout of the pixels in the "n"th row has finished, similar readout of the "(n+1)"th row is performed. In this way, the readout of the pixels is performed row-by-row from the first row through the last row.

As is described, according to the Second Embodiment, a mechanical shutter is left to be open; and a pulse of a PD reset signal RSCELL2 is applied to the gates of the reset transistors 62 of all the pixels 60 at the same time. Hereby, the electric charge accumulated in the PDs 64 of all the pixels is discharged at the same time; from the instant, the accumulation of electric charge to the PD 64 starts. Additionally, the accumulation of electric charge to the PD 64 ends for the all pixels at the same time by closing the

mechanical shutter. Therefore, the start timing and the end timing of the accumulation of electric charge to the PD 64 for all the pixels agree. Consequently, it is possible to take a photograph with no distortion even if the object is moving.

5 The solid-state image sensing apparatus according to the present invention has been explained using the embodiments, but the present invention is not limited to these embodiments.

For example, according to the First Embodiment, in the timing diagram of the timing production 30 shown in FIG. 8, the timings of
10 pulses of a detection region reset signal RSCCELL and a PD readout signal TRANS are aligned. However, as shown in FIG. 12, it is acceptable that the width of a pulse of a detection region reset signal RSCCELL is wider than the width of a PD readout signal TRANS and that the pulse of the detection region reset signal RSCCELL is
15 applied to the signal detection region 128 shown in FIG. 2 before or after the PD readout signal TRANS. Hereby, it is possible to discharge completely the electric charge accumulated in the PD 122.

Additionally, according to the First Embodiment and the Second Embodiment, as shown in FIG. 13, accumulation of electric
20 charge to the PD 122 (64) starts at the trailing edge of a PD readout signal TRANS and a PD reset signal RSCCELL2 and ends at the time when the mechanical shutter is closed. However, the present invention is not limited to this method.

For example, as shown in FIG. 14, it is acceptable that
25 accumulation of electric charge to the PD 122 (64) starts while the mechanical shutter is still open and that the accumulation ends with a pulse of a PD readout signal TRANS or a row selection signal SELECT.

More specifically, while the mechanical shutter is closed, a
30 pulse of a PD readout signal TRANS is applied to the gate of the readout transistor 124 and electric charge accumulated to the PD 122 is discharged. After that, while the mechanical shutter is open,

accumulation of electric charge to the PD 122 starts, a pulse of a PD readout signal TRANS is applied to the gate of the readout transistor 124 and the accumulation of electric charge to the PD 122 ends. After that, the mechanical shutter is closed.

5 Or, while the mechanical shutter is closed, a pulse of a PD reset signal RSCCELL2 is applied to the gate of the reset transistor 62; and accumulated electric charge to the PD 64 is discharged. After that, while the mechanical shutter is open, accumulation of electric charge to the PD 64 starts. Afterward, a pulse of the row
10 selection signal SELECT is applied to the gate of the row selection transistor 68; and accumulation of electric charge to the PD 64 ends. After that, the mechanical shutter is closed.

Like this, a method for ending accumulation of electric charge to PD 122 (64) by a pulse is effective when the mechanical shutter
15 cannot be closed instantly.

Additionally, as is shown in FIG. 15, it is acceptable to control electric charge accumulation time to the PD 122 (64) only by a pulse, not using the mechanical shutter. This method is effective when the mechanical shutter cannot be opened or closed instantly.

20 Further, as is shown in FIG. 16, it is satisfactory to control electric charge accumulation time to the PD 122 (64) only by opening and closing of the mechanical shutter, not using a pulse. This method is effective when the mechanical shutter cannot be opened or closed instantly.

25 Moreover, according to the First Embodiment, the timings of pulses of a detection region reset signal RSCCELL, which is applied to the gate of the reset transistor 126, and a PD readout signal TRANS are aligned. However, the application moment of the pulse of a detection region reset signal RSCCELL is not necessarily limited to
30 this, but can be anytime before electric charge accumulated in the PD 122 is read out.

FIG. 17 is a diagram showing a pulse timing of a detection

region reset signal RSCCELL in a solid-state image sensing apparatus which controls electric charge accumulation time with a mechanical shutter. FIG. 17(a) shows a timing of opening and closing of the mechanical shutter, wherein the time when the mechanical shutter is open is the electric charge accumulation time to PD 122. As is shown in FIG. 17(b), the PD 122 is reset by applying a PD readout signal TRANS to the gate of the readout transistor 124 before electric charge accumulation to PD122 starts.

As is shown in FIG. 17(c), it is acceptable to apply a pulse of a detection region reset signal RSCCELL after electric charge accumulation time has passed. Hereby, it is possible to start electric charge accumulation immediately after accumulated electric charge to PD 122 is reset by a pulse of a PD readout signal TRANS.

Additionally, as is shown in FIG. 17(d), it is satisfactory that a detection region reset signal RSCCELL is at the High level while the width of the detection region reset signal RSCCELL is wider than the width of a pulse of a PD readout signal TRANS and the PD readout signal TRANS is at the High level. By configuring like this, it is possible to completely discharge electric charge accumulated to the PD 122.

Further, as is shown in FIG. 17(e), it is acceptable to apply a pulse of a detection region reset signal RSCCELL to the gate of the reset transistor 126 before electric charge accumulation time ends. Hereby, it is possible to reset the electric charge leaked from the PD 122 to the signal detection region 128.

Still further, as is shown in FIG. 17(f), it is satisfactory to apply a detection region reset signal RSCCELL, which is at the High level, to the gate of the reset transistor 126 from the time before electric charge accumulation time ends and to the time after the electric charge accumulation time ends. Hereby, it is possible to reset electric charge accumulated in the signal detection region 128 before electric charge accumulated in PD 122 is read out. Hereby,

it is possible to detect the accumulated electric charge in PD 122 accurately.

As is shown in FIG. 18A, a mechanical shutter 84 is set up in front of the pixel unit 112 of the solid-state image sensing apparatus explained above but the configuration is not limited to this. For example, a configuration that a liquid crystal shutter 82 is set up in front of the pixel unit 112, as is shown in FIG 18B, is acceptable. A liquid crystal shutter control unit (not illustrated) is set up in the solid-state image sensing apparatus 110 and the liquid crystal shutter control unit controls penetration of light by applying a predetermined voltage to the liquid crystal shutter. Additionally, a configuration that nothing is set up in front of the pixel unit 112, as shown in FIG. 18C, is also acceptable.

Still further, in the above-mentioned First and Second Embodiments, an NMOS-type transistor is used as a transistor. But it is satisfactory to use a CMOS-type transistor instead of the NMOS-type transistor. By using the CMOS-type transistor, for example, the timing generation circuit 30 shown in FIG. 7 is realized as an equivalent circuit to the circuit shown in FIG. 19.

The timing generation circuit shown in FIG. 19 includes: the first switch 92 that is composed of a CMOS-type transistor through which a detection region reset signal RSCCELL passes in response to activated output of the row scanning shift register 114; and the second switch 94 that is composed of a CMOS-type transistor through which the PD readout signal TRANS passes in response to the activated output of the row scanning shift register 114.

Still further, in the First and Second Embodiments, after electric charge is accumulated to the PD122 (64) for all the pixels at the same time, readout to the column scanning shift resistor 118 is performed for each row. However, it is also acceptable to prepare a frame memory which can accumulate pixel signals that correspond to one frame of the pixel unit 112 in advance and transmit the pixel

signals at once.

Additionally, even if the pixel signals cannot be transmitted to the frame memory at once, it is also acceptable to transmit the pixel signals to the frame memory for each row with extremely high speed
5 which can be negligible compared with electric charge accumulation time and scanning time of one television screen.

Further, it is also satisfactory to read out electric charge accumulated in the PD 122 for all the pixels at once when a pixel has a memory (the signal detection region 128) within the pixel like the
10 pixel shown in FIG. 2.

Moreover, in the First and Second Embodiments, electric charge accumulated in the PDs 122 (64) for all the pixels are reset at once. But it is also acceptable to reset electric charge accumulated in the PDs 122 (64) of pixels in a particular region to be
15 read out at once.

As is described above, the present invention can provide a solid-state image sensing apparatus which can photograph a moving object with no distortion.

In recent years, cellular phones with a function to photograph
20 have been rapidly prevailing. Additionally, fields in which a solid-state image sensing apparatus is used such as a camera which a car is equipped with and a monitor camera have been enlarging increasingly. Therefore, the practical value of the solid-state sensing apparatus according to the present invention is extremely
25 high.